REMARKS

With respect to the current and final Office Action:

In the current and final Office Action dated (mailed) 10/12/2004, claims 1-21, 24-26, 28-35, 38-40, and 52-59 were examined. Claims 1-21, 24-26, 28-35, 38-40, and 52-59 were rejected.

Specifically:

Claims 19, 20, and 24 were "rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,167,484 to Boyer et al."

Claims 1-5, 7-16, 18, 38, 39, 54-56, 58, and 59 were "rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,167,484 to Boyer et al. in view of U.S. Patent 5,265,231 to Nuwayser."

Claims 25, 26, 29, 30, 31, 52, and 53 were "rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,167,484 to Boyer et al."

Claims 28 and 32-35 were "rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,167,484 to Boyer et al. in view of 'Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs' by Ohsawa et al., hereinafter simply Ohsawa."

Claims 1-21, 24-26, 28-35, 38-40, and 52-59 were "rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,167,484 to Boyer et al. in view of U.S. Patent 5,265,231 to Nuwayser further in view of 'Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs' by Ohsawa et al., hereinafter simply Ohsawa."

With respect to this current Reply generally:

Claims 60-67 have been added. Of now pending claims 1-21, 24-26, 28-35, 38-40, and 52-67, claims 1, 11, 19, 25, 32, 38, 52, 61 and 65 are independent claims. Each of these independent claims is addressed below.

With respect to Boyer and Ohsawa generally:

Both Boyer and Ohsawa are directed to technology that involves memory, logic, etc. that are located on a single device. As explained further herein below with regard to individual rejections, it appears that the Office Action does not take this fact into consideration when utilizing Boyer and/or Ohsawa in the various rejections.

With regard to Boyer, the entirety of the Boyer document is directed to components that are located (and methods that take place) on a single device. This is indicated and evidenced at numerous locations throughout Boyer. Examples in Boyer include, but are not limited to: [1] "... in an embedded DRAM device." (Abstract, first sentence); [2] "Generally, the present invention is a method and apparatus for reducing the power consumed by DRAM refresh operations and/or improving the system access (i.e., read/write) operational bandwidth of an embedded DRAM." (Column 5, Lines 8-11); [3] "Therefore, a need exists in the industry for a more intelligent manner of scheduling refresh operations whereby: (1) greater system access bandwidth can be provided by an embedded DRAM device so that more performance can be achieved; and/or (2) less power is

consumed by refresh operations internal to the embedded DRAM integrated circuit." (Column 4, Lines 14-20); and [4] other examples as noted herein below.

With regard to Ohsawa, the Ohsawa document is also directed to devices that include both DRAM and logic. This is evidenced in Ohsawa by, for example: [1] "Optimizing the DRAM Refresh Count for Merged DRAM / Logic LSIs" (the title); [2] "Merged DRAM/logic LSIs are expected to play an important role in the 'system-on-silicon' era." (Page 82, Left Column, Section 1: Introduction, First Sentence); [3] "It might be necessary to reconsider refresh architectures for DRAM of merged DRAM/logic LSIs." (Page 82, Right Column, First Sentence); and [4] other examples as noted herein below.

Hence, neither Boyer nor Ohsawa are appropriate for anticipation rejections against memory systems that are distributed on different devices. Furthermore, as explained herein below, neither Boyer nor Ohsawa are appropriate for obviousness rejections either.

With respect to claim 19:

The current Office Action rejects claim 19 solely based on Boyer. The current Office Action reads on page 3 at the fourth paragraph, "Boyer's history qualifiers are not located inside his controller 820." It is respectfully submitted, however, that the relevancy of this assertion is not readily apparent, at least given the applied art of Boyer and the element(s) of claim 19.

For example, claim 19 recites, *inter alia*, **wherein the use registers are not implemented on a same device as the memory cells.** Moreover, as explained

herein above in the sub-section entitled "With respect to Boyer and Ohsawa generally", Boyer cannot anticipate any claim in which all of the elements are not confined to a single device.

Consequently, it is respectfully submitted that no art of record, either alone or in any combination, anticipates or renders obvious at least the following elements in conjunction with the other elements of their respective claim(s):

With respect to claim 19: **one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are configurable to indicate whether the corresponding groups of memory cells are in use . . . wherein the use registers are not implemented on a same device as the memory cells.**

With respect to claims 1, 11, and 38:

The current Office Action rejects claims 1, 11, and 38 based on a combination of Boyer and Nuwayser. The current Office Action reads on page 5 at the second, third, fourth, and fifth paragraphs:

> Boyer's refresh logic omits refreshing of memory cells that are not in use as claimed (column 5, lines 14-19, column 7, lines 46-51).
>
> Boyer's history qualifiers are not located inside his controller 820.
>
> Nuwayser shows a memory controller 14A in Fig. 1 as 14i in Fig. 2. This memory controller includes DRAM control circuit 23 which includes refresh register circuit 41, detailed in Fig. 3 and discussed at column 6, line 44 through column 7, line 31. Refresh registers 41 include refresh flags for each memory bank controlled by that particular controller.

> It would have been obvious to one of ordinary skill in the art at the time the invention was made *to implement Boyer's history decoder 804 (which includes the history qualifiers 808) inside system DRAM controller 820* because Boyer shows the history qualifiers in different locations in different embodiments (in Fig. 8 they are separate from the memory devices while in Fig. 2 they are in the memory devices, as taught at column 14, lines 48-56) clearly indicating that the history qualifiers are not restricted to a single location and furthermore because Nuwayser shows refresh register flags stored in his memory controller 14i, clearly teaching consolidation of all refresh control circuitry within the memory controller.
>
> [italicized emphasis added]

First, it is respectfully submitted that both of the history decoder 804 and the system DRAM controller 820 of Boyer are located on a single device and would have remained so even given the asserted combination of Boyer and Nuwayser as expressed in the Office Action.

Second, it is respectfully submitted that Boyer could not have been combined with Nuwayser for any purpose because there is insufficient motivation to combine them. Furthermore, even assuming, *arguendo*, that Boyer could have been combined with Nuwayser for some purpose, it is respectfully submitted that any such hypothetical combination would not have resulted in the claimed invention.

Moreover, it is respectfully submitted that Boyer *teaches away from* any combination with Nuwayser (and/or any other art with different discrete component devices). Boyer is directed to addressing problems that arise only when DRAM is incorporated on the same device as other components. Consequently, Boyer teaches that utilizing one or more of the approaches

described in Boyer only serves to introduce additional costs, complexities, and other overhead into Nuwayser without having any purpose, much less any benefit.

Examples of *teachings away from* any combination of Boyer and Nuwayser in the Boyer document include, but are not limited to:

> It should now be clear that timely performance and/or intelligently performing DRAM refreshes in embedded DRAMs becomes a serious concern whereas discrete DRAM devices are not concerned with improving refresh consumption of bandwidth since the bandwidth consumed in discrete DRAMs is insignificant.
>
> (Boyer, Column 2, Lines 42-47.)

> Discrete DRAM refresh operations, as are known in the art, are not intelligent refresh operations and do not need to be intelligent since the operational impairment and power consumption of refresh operations in a discrete DRAMs are generally not thought to be of big concern. In other words, since the bandwidth consumed by refresh operations in a discreet DRAM is less than 1% of the total bandwidth, there is little to be gained in complicating the design of a discrete DRAM device to perform intelligent refresh operations.
>
> (Boyer, Column 2, Line 61 to Column 3, Line 2.)

> In the discrete DRAMs, refreshes are performed with no intelligent processing of the access history or operational states of the memory rows. While the added power and reduced bandwidth is not a problem for discrete DRAMs as shown above, this added power and lost bandwidth would be severely degrading to the performance of an embedded DRAM device.
>
> (Boyer, Column 3, Lines 27-33)

As is apparent from the portions of Boyer that are reproduced above, Boyer actually *teaches away from* any combination of Boyer with Nuwayser. Consequently, it is respectfully submitted that the obviousness rejection under 35 U.S.C. §103(a) that is applied to claims 1, 11, and 38 is improper under both the

relevant facts and the applicable law. Accordingly, withdrawal of the rejection(s) against claims 1, 11, and 38 is respectfully requested.

Thus, for either or both of the reasons given above, it is respectfully submitted that no art of record, either alone or in any combination, anticipates or renders obvious at least the following elements in conjunction with the other elements of their respective claims:

With respect to claim 1: **refresh logic to refresh memory cells of at least one memory device . . . the memory controller comprises at least part of a device other than the at least one memory device.**

With respect to claim 11: **a plurality of memory devices having memory cells; and a memory controller on a different device including one or more dynamically changeable use registers . . . .**

With respect to claim 38: **periodically refreshing memory cells located at one or more memory cell devices; receiving internal notifications regarding which memory cells are in use based on data stored in a plurality of use registers located on another device including the memory controller.**

With respect to claims 25, 52, 61, and 65:

The current Office Action rejects claims 25 and 52 based on Boyer and information that is asserted to be "notoriously well-known". The current Office Action reads over two paragraphs starting on page 3 at the fourth paragraph:

> Regarding claims 25, 26, 52, and 53, Boyer does not explicitly disclose the claimed operating system, however it is inherent in his device as the

> controlling software running on the processor which is not shown in his figures. Clearly, the processor must have an operating system and it allocates and deallocates memory based on memoy mapping portions being active or inactive, as claimed.
>
> Boyer also does not disclose using virtual-to-physical memory mapping, but this was notoriously well-known at the time of the invention as the preferred method of memory management, with the operating system using virtual memory to provide the processor with a large address space without having to provide the equivalent amount of physical memory. As various virtual pages are needed, they are paged or swapped in and out of the physical memory.

First, as explained herein above in the sub-section entitled "With respect to Boyer and Ohsawa generally", Boyer is directed to embedded systems. Embedded systems do not typically require or include secondary memories. Hence, there would be insufficient motivation, if any, to incorporate a virtual memory mechanism, along with the attendant processing overhead, into the embedded systems of Boyer.

Second, and more importantly, the rejections of claims 25 and 52 in the current Office Action do not address all of the elements of these claims. For example, claim 25 recites, *inter alia*, **an operating system configured . . . to identify allocated and de-allocated memory to the memory controller**. Even assuming, *arguendo*, (i) that an embedded system of Boyer includes an operating system and (ii) that it would have been modified by one of ordinary skill in the art at the time of the invention to incorporate a virtual memory mechanism, claim 25 would nevertheless not have been rendered obvious.

Specifically, but by way of example only, there is no suggestion in Boyer, in another document of record, or in the knowledge of the art generally, to modify

the asserted hypothetical virtually-memory-mechanism and operating system of Boyer such that, e.g., de-allocations are identified to the memory controller.

Thus, for either or both of the reasons given above, it is respectfully submitted that no art of record, either alone or in any combination, anticipates or renders obvious at least the following elements in conjunction with the other elements of their respective claims:

With respect to claim 25: **an operating system configured to dynamically allocate and de-allocate the memory and to identify allocated and de-allocated memory to the memory controller based on whether or not virtual-to-physical memory mapping portions are active.**

With respect to claim 52: **A method for a memory device comprising: receiving at the memory device memory allocation and de-allocation notifications from an operating system.**

With respect to claim 61: **A memory device that is capable of receiving memory de-allocation notifications from an operating system.**

With respect to claim 65: **receiving at the memory device memory allocation and de-allocation notifications from an application.**

<u>With respect to claim 32:</u>

The current Office Action rejects claim 32 based on a combination of Boyer and Ohsawa. The current Office Action reads on page 9 at the first

sentence, "Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2."

On page 85 in Section 3.2, Ohsawa reads in pertinent part, " . . . the system which provides a write-back cache can stop refreshing to a row if all cache lines of the row would became dirty (see Figure 6). This is because each of these cache lines will be written back inevitably." As indicated in Figure 6, Ohsawa stops refreshing the DRAM only after a write to the cache system.

Hence, it is respectfully submitted that no art of record, either alone or in any combination, anticipates or renders obvious at least the following elements in conjunction with the other elements of their respective claim(s):

With respect to claim 32: **indicating that memory rows, upon being transferred to a cache, are not in use prior to when the transferred memory rows are written-to in the cache.**

With respect to the dependent claims:

Reasons for the allowability of independent claims 1, 11, 19, 25, 32, 38, 52, 61, and 65 have been provided above. Although each pending dependent claim also includes additional element(s) militating toward allowability, the dependent claims are allowable at least for the reasons given above in connection with their respective independent claims.

CONCLUSION

It is respectfully submitted that all of claims 1-21, 24-26, 28-35, 38-40, and 52-67 are allowable, and prompt action to that end is hereby requested.

Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

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